AN1606
APPLICATION NOTE

A "BRIDGELESS P.F.C. CONFIGURATION" BASED ON L4981 P.F.C. CONTROLLER.

by Ugo Moriconi

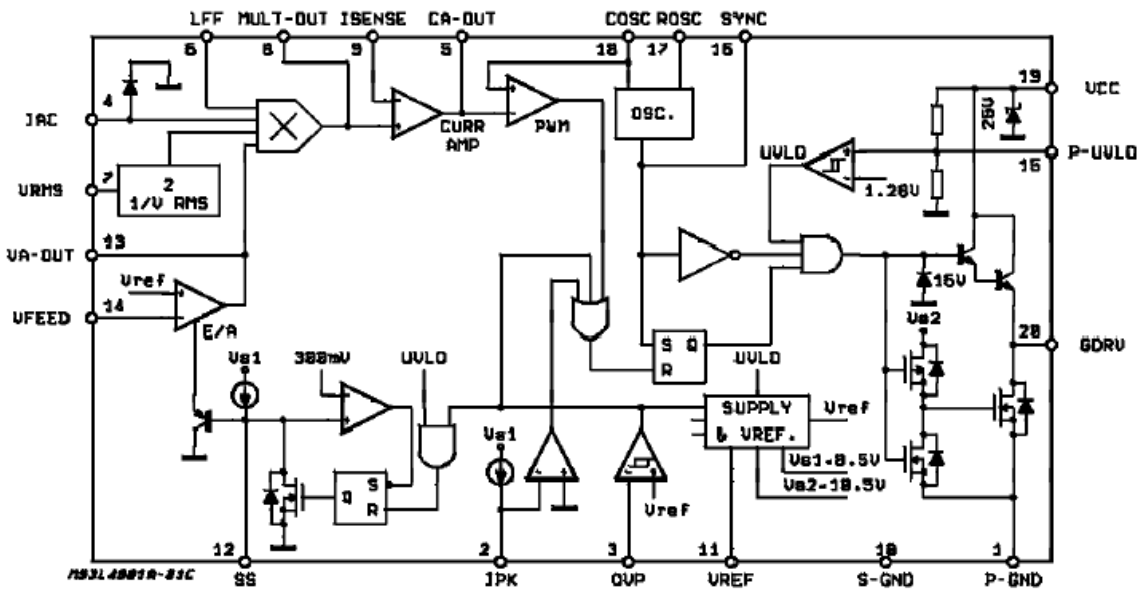
This technical document describes an innovative topology dedicated to a medium to high power PFC stage. The originality of this topology is the absence of the bridge that usually is placed between the EMC filter and the PFC stage. The advantages of this topology can be found in terms of increased efficiency and improved thermal management.

L4981 PFC Controller

This application features the L4981 PFC controller. It is a high performance device operating in average current mode with many on-chip functions. The driver output stage can deliver 1.5A, which is very important for this type of application.

A detailed device description can be found in AN628. A functional block diagram is shown in Figure 1.

Figure 1. Functional Diagram

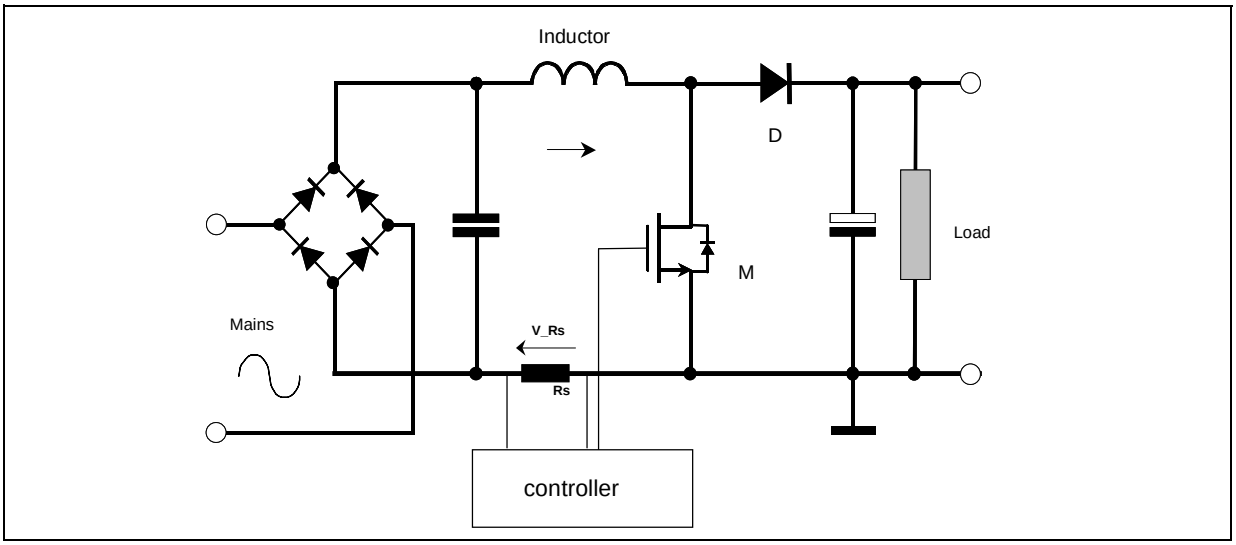


Description of "Bridgeless PFC Configuration" Topology

The conventional boost topology is the most efficient for PFC applications. It uses a dedicated diode bridge to rectify the AC input voltage to DC, which is then followed by the boost section. See Figure 2.

This approach is good for a low to medium power range. As the power level increases, the diode bridge begins to become an important part of the application and it is necessary for the designer to deal with the problem of how to dissipate the heat in limited surface area. The dissipated power is important from an efficiency point of view.

Figure 2.

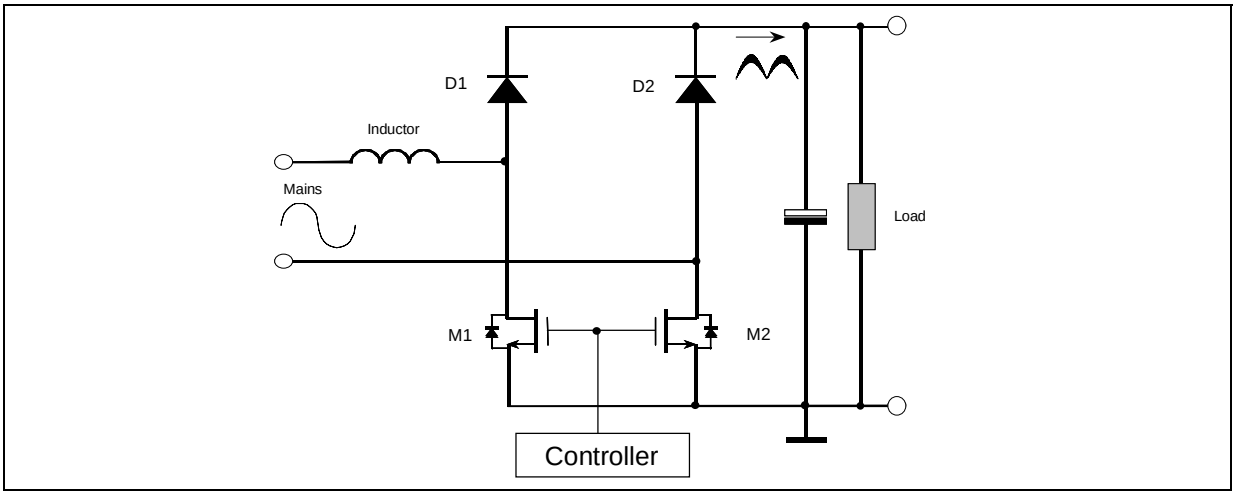


The bridgeless configuration topology presented in this paper avoids the need for the rectifier input bridge yet maintains the classic boost topology.

This is easily done by making use of the intrinsic body diode connected between drain and source of PowerMOS switches.

A simplified schematic of the bridgeless PFC configuration is shown in Figure 3.

Figure 3.

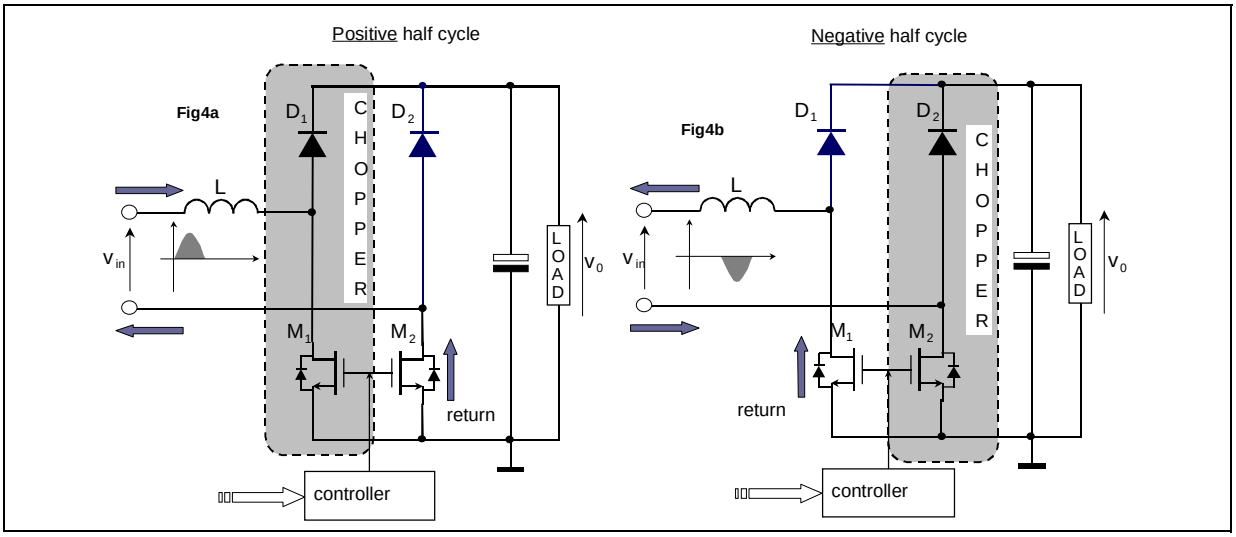


The circuit shown from a functional point of view is similar to the common boost converter. In the traditional topology current flows through two of the bridge diodes in series. In the bridgeless PFC configuration, current flows through only one diode with the PowerMOS providing the return path.

To analyze the circuit operation, it is necessary to separate it into two sections. The first section operates as the boost stage and the second section operates as the return path for the AC input signal.

Referring to Figure 4, the left side (Figure 4a) shows current flow during the positive half cycle and the right side (Figure 4b) shows current flow during the negative half cycle

Figure 4.



Positive "HALF Cycle."

When the AC input voltage goes positive, the gate of M1 is driven high and current flows from the input through the inductor, storing energy. When M1 turns off, energy in the inductor is released as current flows through D1, through the load and returns through the body diode of M2 back to the input mains. See Figure 4A

During the-off time, the current throw the inductor L (that during this time discharges its energy), flows in to the boost diode D1 and close the circuit through the load.

Negative "HALF Cycle".

During the negative half cycle circuit operation is mirrored as shown in Figure 4B. M2 turns on, current flows through the inductor, storing energy. When M2 turns off, energy is released as current flows through D2, through the load and back to the mains through the body diode of M1.
Note that the two PowerMOSFETs are driven synchronously. It doesn't matter whether the sections are performing as an active boost or as a path for the current to return. In either case there is benefit of lower power dissipation when current flows through the PowerMOSFETs during the return phase.

Current Sensing.

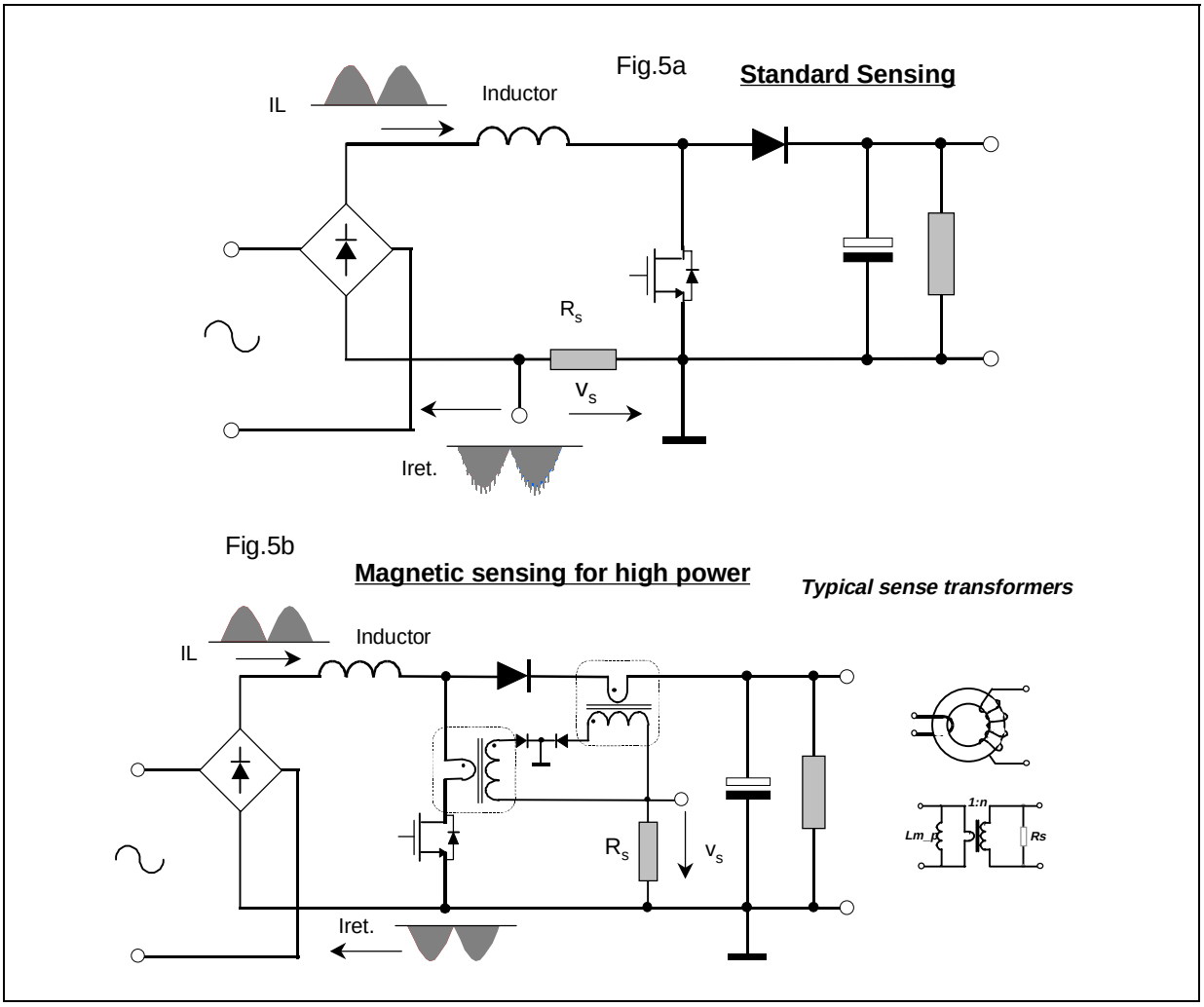
The PFC function requires controlling the current drawn from the mains and shaping it like the input voltage waveform. To accomplish this it is necessary to sense the current and feed its signal to the control circuit.
In average current conventional boost topology, we sense the rectified current rather than the AC input current. This can be achieved by a simple sensing resistor in the return of the current to the bridge, as shown in Figure5a.

The L4981A/B current loop is designed to handle this negative signal. This type of resistor current sense can easily be achieve in medium power applications. For high power PFC circuits it is necessary to use a magnetic current transformer for improved efficiency as shown in Figure 5b.

In the bridgeless PFC configuration since an input rectifier bridge is not used, the current is continuously changing its direction and the complexity of current sensing with a simple resistor can increase. Also in high power applications, resistor sensing may dissipate too much power. In these cases, current sensing with a current transformer is the preferred approach.

A current sense transformer core is typically high permeability ferrite (toroidal or a small core set). The primary of the transformer is a single turn of wire through the core. The secondary typically consists of 50 to 100 turns.

Figure 5. .



This type of sense transformer cannot operate at low frequency and for this reason it must be connected where the current is switched at high frequency. The magnetic core must be allowed reset.
This is normally accomplished by using a diode. In order to reproduce the inductor's current in boost topology, two of magnetic sense sections are needed and the simplified schematic is shown in figure 5b.

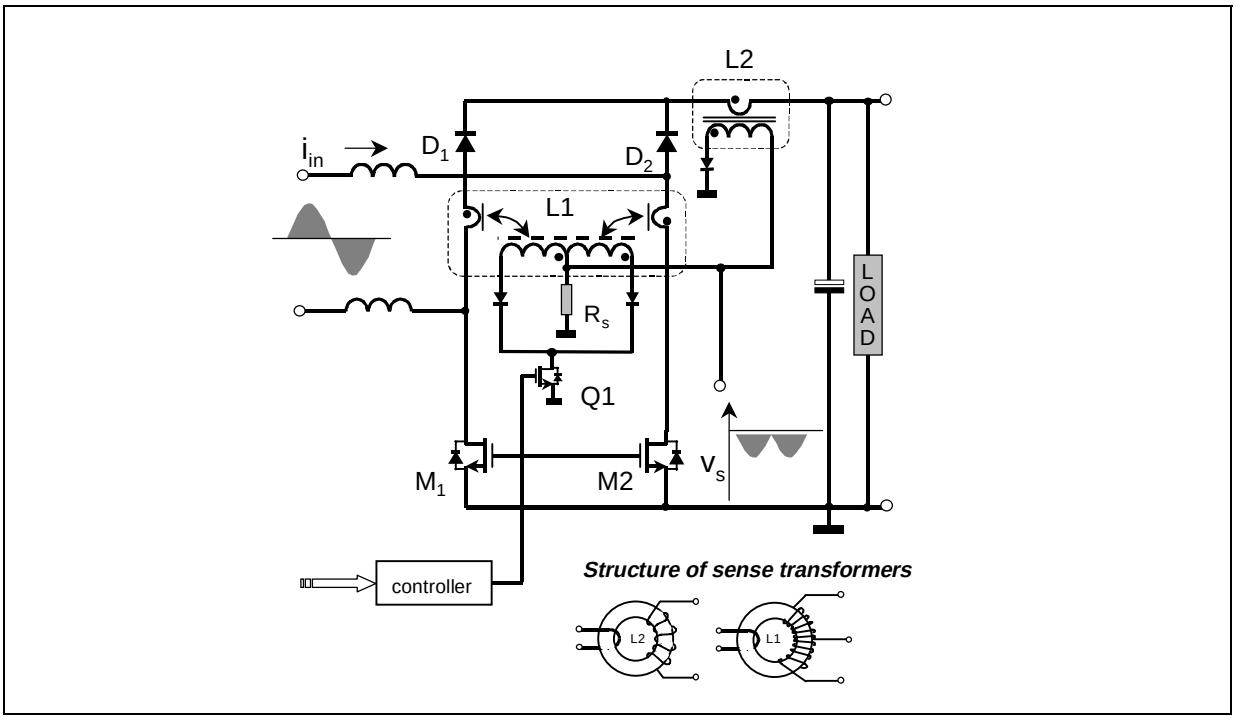
When the sense transformer solution is applied in the bridgeless topology, the simple sense as in fig5b, is no longer valid.

The circuitry is more complex than in the boost case because here we have two pair of PowerMOS (M1, M2) and diodes (D1, D2) alternating.

It is necessary to sense the chopping current of the (PowerMOS + diode) section and to sum the signals to be applied to Rs.

The sensing of the diode's current can be simply done by placing a magnetic sensor at the common cathode (L2 in fig.6.). Only one of the two diodes operates each half input cycle.

Figure 6.



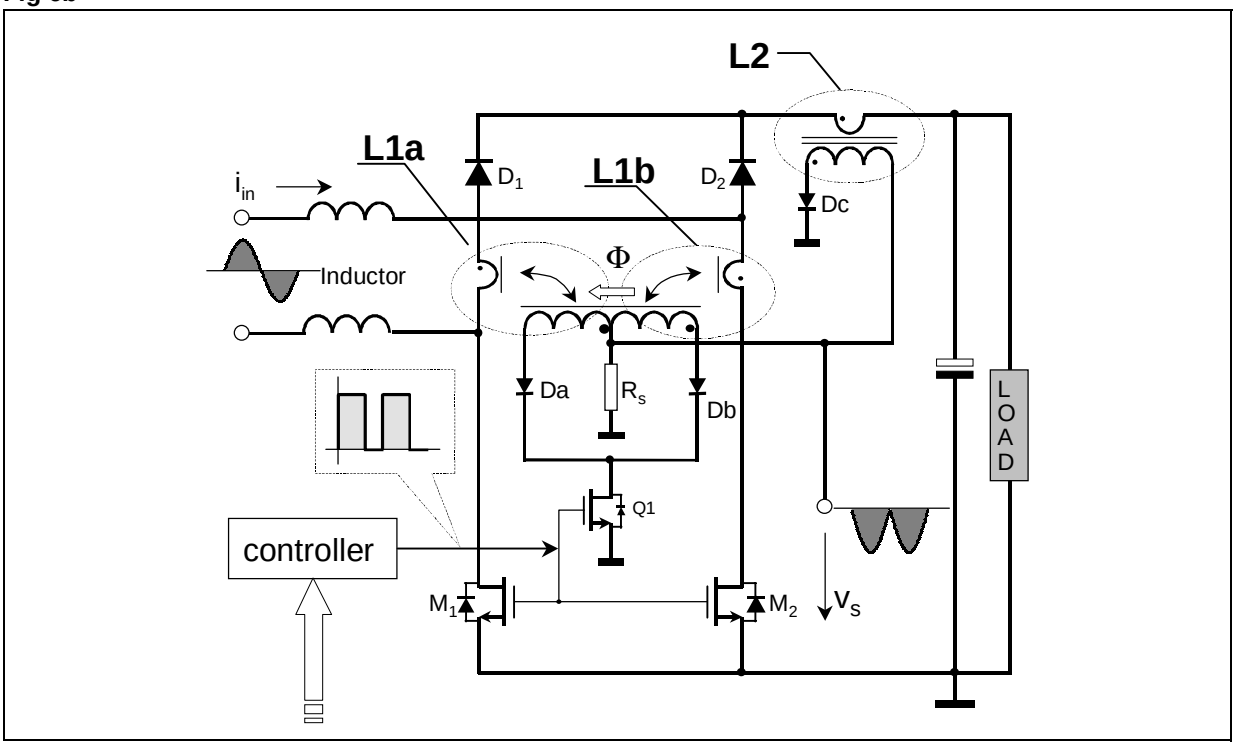
For the PowerMOSFET portion of the circuit, the complexity increases because during the half cycle when one of the PowerMOSFETs is chopping, the other one has to handle the current flowing back to the mains.

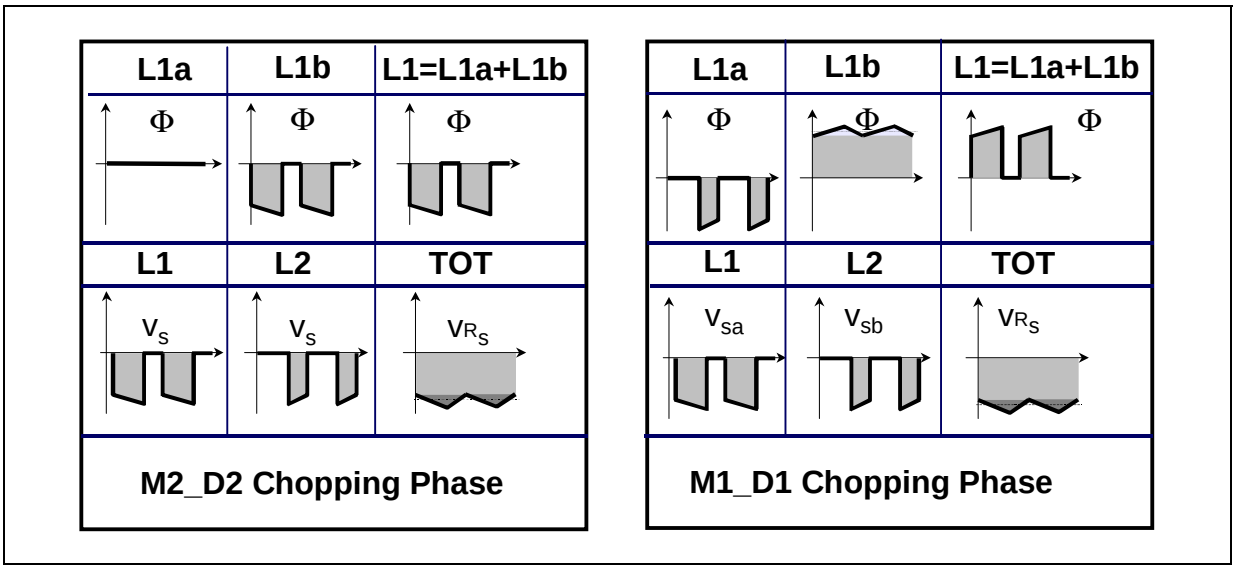
Using the configuration of sensors as shown in Figure 6 it is possible to solve the problem without undue complexity. The unnecessary high frequency portion of the current signal is cancelled because of the method M1 is connected to L1A as shown in Figure 6b. The problem due to the change of polarity during each half cycle is solved by using a center tapped secondary and two rectifiers.

Since the coupling of the two windings must not permit the demagnetization of L1, an auxiliary transistor Q1 is used that opens the circuit during the off-time. For the L4981 controller, the off-time is guaranteed not to be less than 5% of the period. Q1 can be a small signal transistor because its switched current is low due to the fact that the transformer secondary will have a large number of turns.

To realize the current sensing transformer, a high permeability toroidal core (ur=>5000) has been used. The secondary has 50 turns as a compromise to reduce secondary current yet not require a large number of turns.

Fig 6b



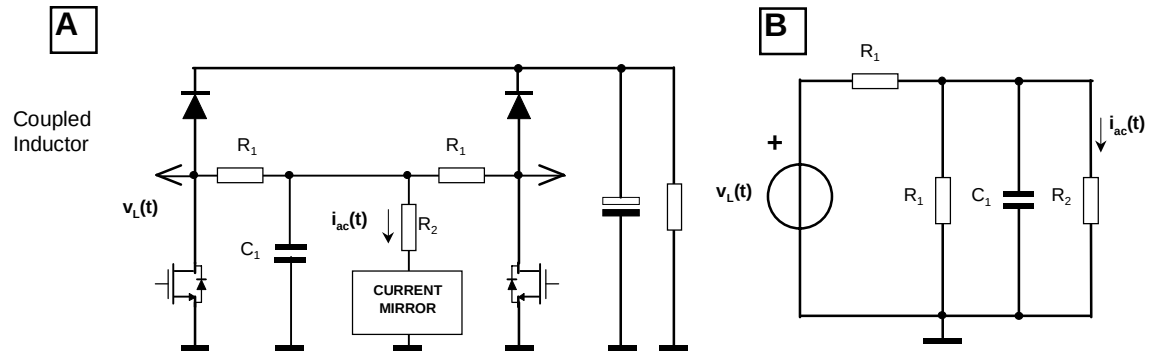


Other control circuits

Input voltage sensing: in the standard boost topology the rectified input voltage waveform is sensed using a resistor that, by one internal circuit, delivers the mirrored signal to one of the multiplier's inputs (Iac-pin4).

For the bridgeless configuration see the circuit shown in fig.7.

Figure 7.



Input voltage sensing (A), and equivalent circuit (B).

It is based on the following consideration: the frequency of the signal of interest (tens of Hz), is much lower than the switching frequency (tens of kHz). The boost inductor, for the low frequency, behaves like a short circuit. Since the Powermos's drains are, in turns, close to ground (via the body diode), the resulting equivalent circuit is shown in fig7b.

The relation between the voltage (from the inductor) and the current that flows in to Iac pin is:

a) $Y(s) = \frac{1}{Req} \cdot \frac{1}{1 + st}$

Where: $Req = R1 + 2 \cdot R2$ and $t = \left[\frac{R1}{2} // R2\right] \cdot C1$

The net introduces one pole at: $fp = \frac{1}{2 \cdot \pi \cdot t}$

The pole must be located at a frequency high enough not to distort the input waveform and at the same time, low enough to filter the switching frequency.

In this application the equivalent resistance has been choosen

Req.=324-kΩ that fits well with the current amplifier design.

The resulting R1 is 300kΩ and R2 is 12kΩ

The pole has been placed a decade before the switching frequency:

Fp = 5kHz that gives:

b) $C1 = \frac{1}{2 \cdot \pi \cdot fp \cdot \left(\frac{R1}{2} // R2\right)} = 2.87nF$

In practice, in our test, a standard value of 2.7 nF as ben used.

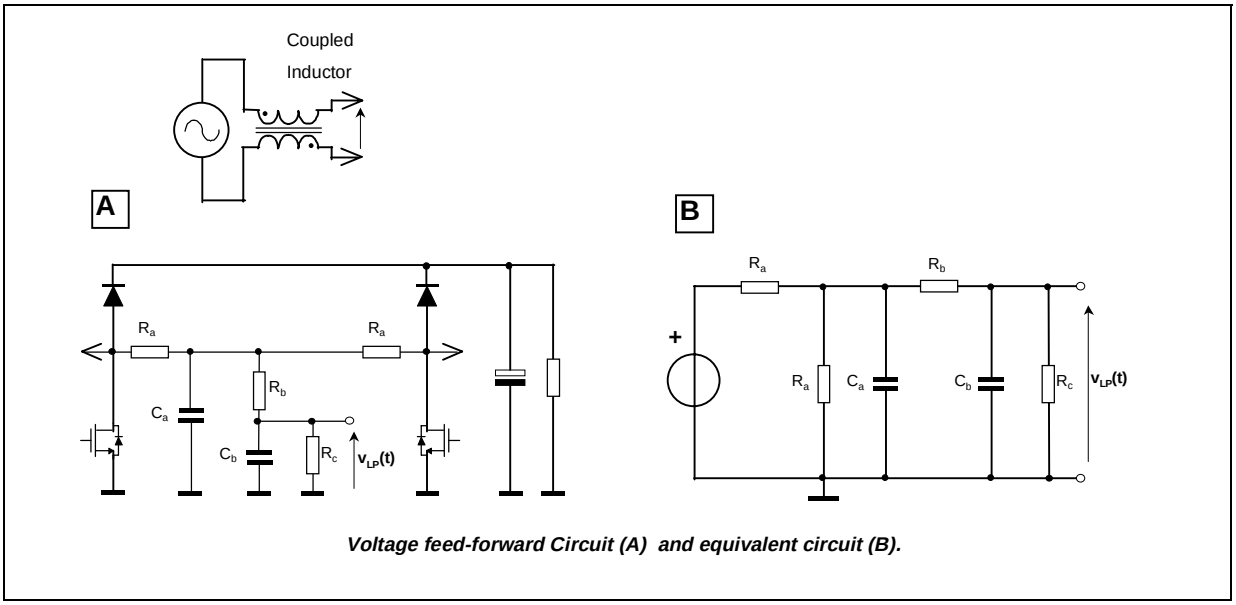
Voltage feed-forward.

Voltage feed-forward, a useful function in wide range applications, requires a DC voltage proportional to the rms. value of the input mains. For the L4981, this value must be between 1.5V to 5.5V so that it can mirror over a wide range.

Since the rectified mains frequency is 100 -120Hz, we need a large rejection for this frequency and because the feed-forward reaction time is proportional to the bandwidth, we introduce a second order filter that allows good compromise between attenuation of the fundamental frequency and response time.

The circuit (Fig.8) is similar to the fig.7 described earlier.

Figure 8.



Voltage feed-forward Circuit (A) and equivalent circuit (B).

Defining $H_{LP}(s)$ the transfer functions between the voltage from the inductor and the voltage at the output of the filter v_{LP} (Fig.8B), we have the following relation:

c) $$H_{LP} = K_{LP}\frac{1}{(1+st_1)\cdot(1+st_2)} \qquad K_{LP} = \frac{R_c}{(Ra+2Rb+2Rc)}$$

The time constants cannot be expressed in simple way and so that the position of poles can be numerically calculated.
The constant K_{LP} is defined taking in to account the wide-range that is, V_mains is between 88V and 264V:

d) $$V_{LP} = V_{RMS}\frac{2\sqrt{2}}{\pi}\cdot K_{LP}$$

Choosing to calculate this value at the midpoint of the allowed values:

e) $$\frac{2\sqrt{2}}{\pi}\cdot\frac{88+264}{2}\cdot K_{LP} = \frac{1.5+5.5}{2}$$

To fit this, it has been choosen

$$\begin{pmatrix} Ra = 998k\Omega \equiv (2 \cdot 499) \\ Rb = 150k\Omega \\ Rc = 30k\Omega \end{pmatrix}$$

For the capacitors, we set 80 dB of attenuation on the fundamental frequency using the commercial values: -

$$\begin{pmatrix} Ca = 390nF \\ Cb = 470nF \end{pmatrix}$$

The design places two poles at 3Hz and 14Hz and 80 dB of attenuation at 100Hz.

Practical examples.

The preceeding points of this note have described the topology peculiarity. Remainder of the topics, for PFC design, are similar to standard P.F.C. boost applications based on L4981A/B (see the related references and application notes).

Starting from now, we can refer to real design examples.

In fact, in order to verify the efficacy of the described configuration, it have been checked a pair of application's size. For evaluation porpoise, it has been realized a printed circuit.

Let us beginnes with and 800W P.F.C application.

800W Target:

1 - Wide range input voltage variation 110Vrms to 220Vrms.

2 - Output power 800W.

2 - Output voltage 400Vdc.

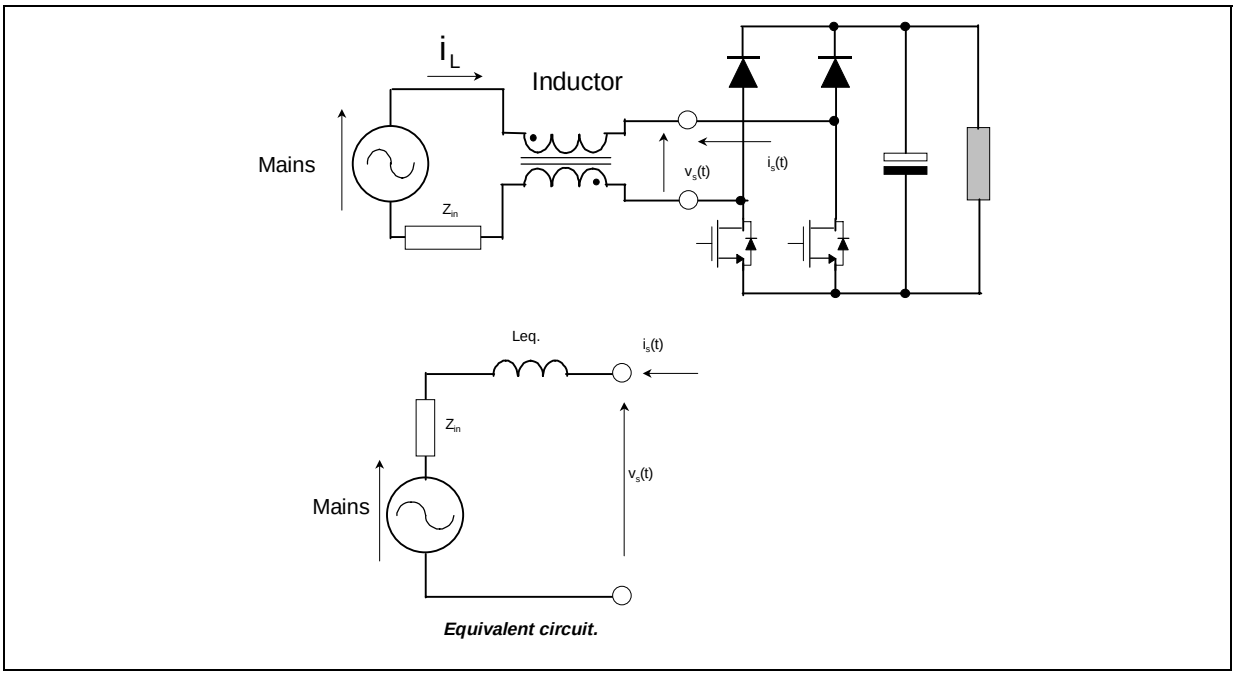
A switching frequency of 50 kHz has been chosen as a good compromise between the coil-size and the powerMOS switching losses.

Boost Inductor design.

To design the boost inductor, the parameters under consideration are the percentage current ripple (as low as possible) and the cost of the bobbin. This portion of the design is the same as for the standard topology.

In this application, in place of a single inductor connected to one of the phases, it has been chosen to split the inductor into two sections (two windings on the same core) as shown in the connection diagram at fig.9.

Figure 9. Connection Diagram for the Coupled Inductor



Equivalent circuit.

Realizing the inductor in this manner improves common mode rejection and avoids the effect of the difference between drain capacitance of the PowerMOSFETs. In order to simplify the model, assume a near unity coupling factor and the equivalent circuit is shown in Figure 9b.

The inductance is proportional to the square of the number of turns. For the two windings it will be:

f) $N' = \frac{N}{2}$ and

$$N' \text{ total} = \frac{N}{2} + \frac{N}{2}$$

The required number of turns for a given inductance on the same core is the same as it is for one winding or two windings. The only difference is that the two windings are separated into two sections. For simplicity we can design the coupled inductor using the same criteria as for a standard inductor - core size, number of turns, and size of copper wire.

For the core, the preferred design is a gapped ferrite core set.
The size of the core can be chosen considering the maximum current Ipk. that, for the 800W target's parameters can exceed 14A (placing Ipk. = 15A).

g) $V_{core} \geq V_{core,""min} = K \cdot L \cdot I^2 peck \quad (mm^3)$

Where: $K = 1.4 \cdot 10^4 \cdot \frac{lcore}{lgap}$

For the 800W application, the nominal current ripple has been chosen around 25%. This fixes the boost inductance value L=450µH.

The coil requirements can be met using a gapped core set type E66/33/27, characterized with the following key parameters:

Ae = 550mm^3; lcore = 146mm; m_core = >1600;

Vcore = 80.4*10^3mm^3

The air gap needed to avoid saturation and optimize the coil size is equal to lap = 3mm.

Using the parameters in the formula g).

Vcore>67.5mm^3

This result confirms the core is well above the minimum size.

The used formula for the number of turnes, needed to design the total required inductance L, is:

h) $$N = \sqrt{\frac{L}{\mu_0} \cdot \left[\frac{l, core}{\mu_r, core \cdot A} + \frac{1gap}{\left(\sqrt{A + \frac{\pi}{4} \cdot 1gap} \right)^2} \right]}$$

The resulting N=38, in our solution, has been realized with 19 turns +19 turns.

In order to minimize the high frequency losses, the winding has been made using the "multiple wire" approach. It is possible to estimate the losses for a low frequency current.

Imposing a maximum power value to be dissipated in the copper (Pcu = 5W)

i) $$P_{wire} = R_{DC} \cdot I^2_{RMS, max} < 5W \qquad R_{DC} < \frac{P_{wire}}{I^2_{RMS, max}} = 60m\Omega$$

Using the formula for multiple wires: -

l) $$R_{DC} = \rho_{Cu} \cdot \frac{l_{turn} \cdot N}{\frac{\pi}{4} \cdot d^2 \cdot M} < 60m\Omega$$

Were:

In practice 20 wires were used, each having a diameter d=0.4 mm.

Output Capacitor filter.

For the bulk capacitor selection, we consider a reasonable 100Hz voltage ripple.

m) $$Co = \frac{Po}{2 \cdot \pi \cdot 2 \cdot f \cdot \Delta fo \cdot Vo}$$

were f is the input frequency.

Imposing <10Vac the peak of voltage variation over 400Vo, the Co value will results >318µF; the commercial value is 330µF

Power Devices.

The selection of the power devices is dependent upon the topology and the size of the application.

Operating in continuous current mode, fast reverse recovery diodes are needed.

The TURBOSWITCH "STM family", in the 600V voltage range, offers a very good solution for the two boost diodes, the STTH8R06FP has been chosen.

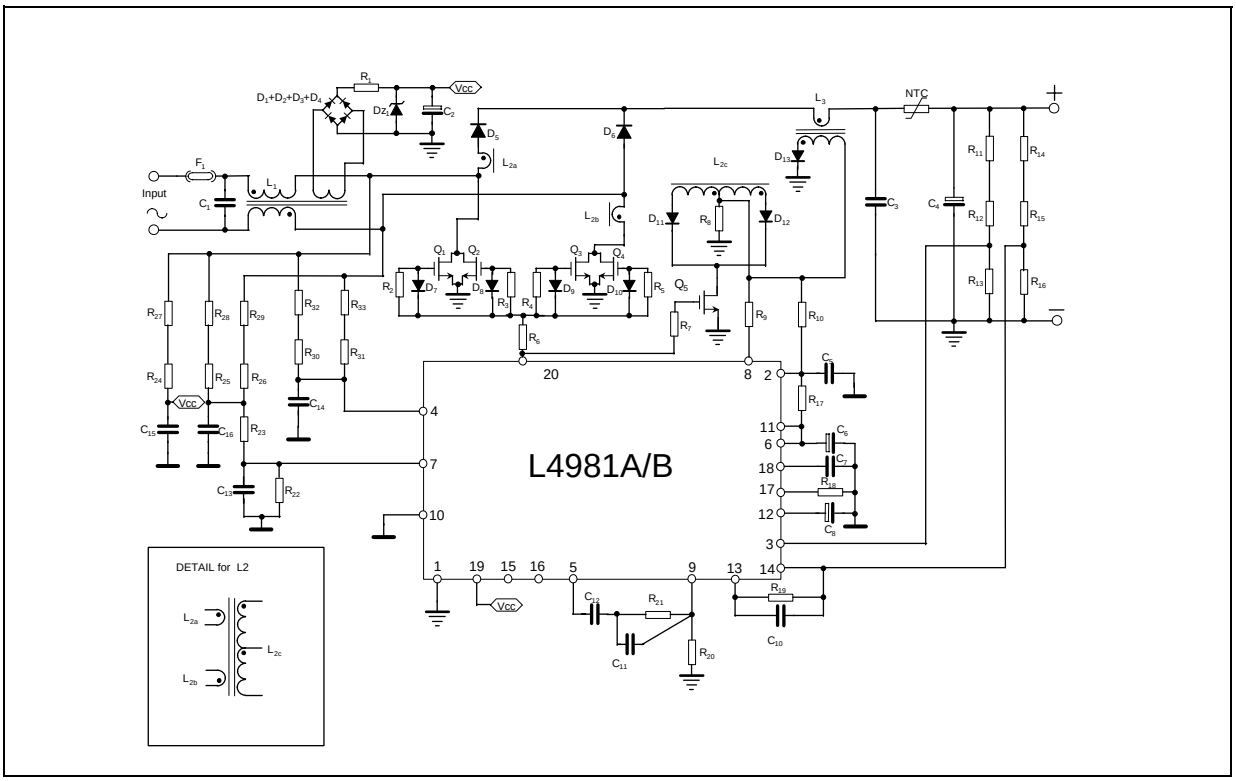
The insulated TO-220 package makes it easy to assemble the parts on a heat sinke.

Concerning the Powermos requirements, a 500V blocking voltage (Bvdss) is needed, for this application.

The chip selection is more complex. To find the best solution, it must be considered all the parameters that affect the power dissipation and to compare the results in terms of a cost to benefit ratio. The devices used in the 800W application (2+2), are the type STY34NB50F.

The four Powermos are efficiently driven without any additional buffer, thanks to the smart characteristics of the integrated driver.

Figure 10. 800W SCHEMATHIC DIAGRAM.



B.O.M. for 800W Bridgeless Evaluation Circuit.

Name	Value	Name	Value	Name	Value	Name	Value	Name	Value
R_1	68 Ω	$R_{2,3,4,5}$	10 Ω	R_6	1.8 Ω	R_7	100 Ω	R_8	5 Ω
R_9	2.7 kΩ	R_{10}	1.5 kΩ	$R_{11,12,14,15}$	1 MΩ	R_{13}	22 kΩ	R_{16}	25.5 kΩ
R_{17}	3.9kΩ	R_{18}	27 kΩ	R_{19}	220 kΩ	R_{20}	2.7 kΩ	R_{21}	5.6 kΩ
$R_{22,24,27}$	30 kΩ	$R_{23,30,31,32,33}$	150 kΩ	$R_{25,26,28,29}$	499 kΩ	R_{34}	12 kΩ	RSN	12 Ω
$C_{1,3}$	1 µF	C_2	220 µF	C_4	330 µF	C_5	10 nF	C_6	1 µF
C_7	1.8 nF	C_8	1 µF	C_{10}	120 nF	C_{11}	1 nF	C_{12}	5.6 nF
C_{13}	470 nF	C_{14}	2.7 nF	C_{15}	100 nF	C_{16}	390 nF		
NTC	2.5	B57364		F1	20A				

$L_{2,\#(1/50+50)}$# sense transformer; $L_{3\#(1/50)}$# sense transformer

#Ferrites Hy_perm.' Diam.=20mm

$D_{1,2,3,4}$; $D_{7,8,9,10,11,12,13}$ = 1N4148 ; Dz_1 = 1N4746; Q_5 = BS170

L_1=450 µH; => E66*33*27-18+18 turns 3mm/gapped# 20 wires //m=0.4 mm each.

$D_{5,6}$ = STTH8R06FP; $Q_{1,2,3,4}$=STY34NB50F

Note: For the evaluation circuit and external coupled inductor EMC where utilized.

The filter has been achieved as follows: -

Coupled inductor (30 + 30) turns; wire diameter = 0.8mm on a toroidal (40x17x9 mm): -

Magnetizing inductance (each half inductor) Lm=8mH and a leakage inductance, Ld=50µH.

Scaling down the application.

As a second step, based on the same circuit, a 600W P.F.C. has been built.
The target specification designed for server application is.

600W Target:

1- Wide range input mains 110Vrms to 220Vrms.

2- Output power = 600W.

2- Output voltage = 400Vdc.

The switching frequency has been set at 75kHz to use a reduced size and high performance PowerMOS.

Boost Inductor design.

The boost inductor has been design as been previously described .

For the 600W application, the nominal current ripple has been set around 22%, gives requires the inductance value L=440µH.

The inductor requirements can be met using the core set type E55/28/21, characterized with the following key parameters:

A = 357mm^2; lcore = 123mm; m_core =>1600;

Vcore = 43.7mm^3

The needed air gap is: l_{ap}=2.5mm.

Using the relation g), Vcore>38.8mm^3

The result confirms that the core is good enough.

Using the relation **h)**, the resulting N=42.

For the 600W, the coil has been realized with 21 turns +21 turns.

For minimize the high frequency losses, the "multiple wire" solution has been used.

Imposing the copper losses (Pcu = 3.8W), it has been used 14 wires having a diameter d = 0.4 mm each.

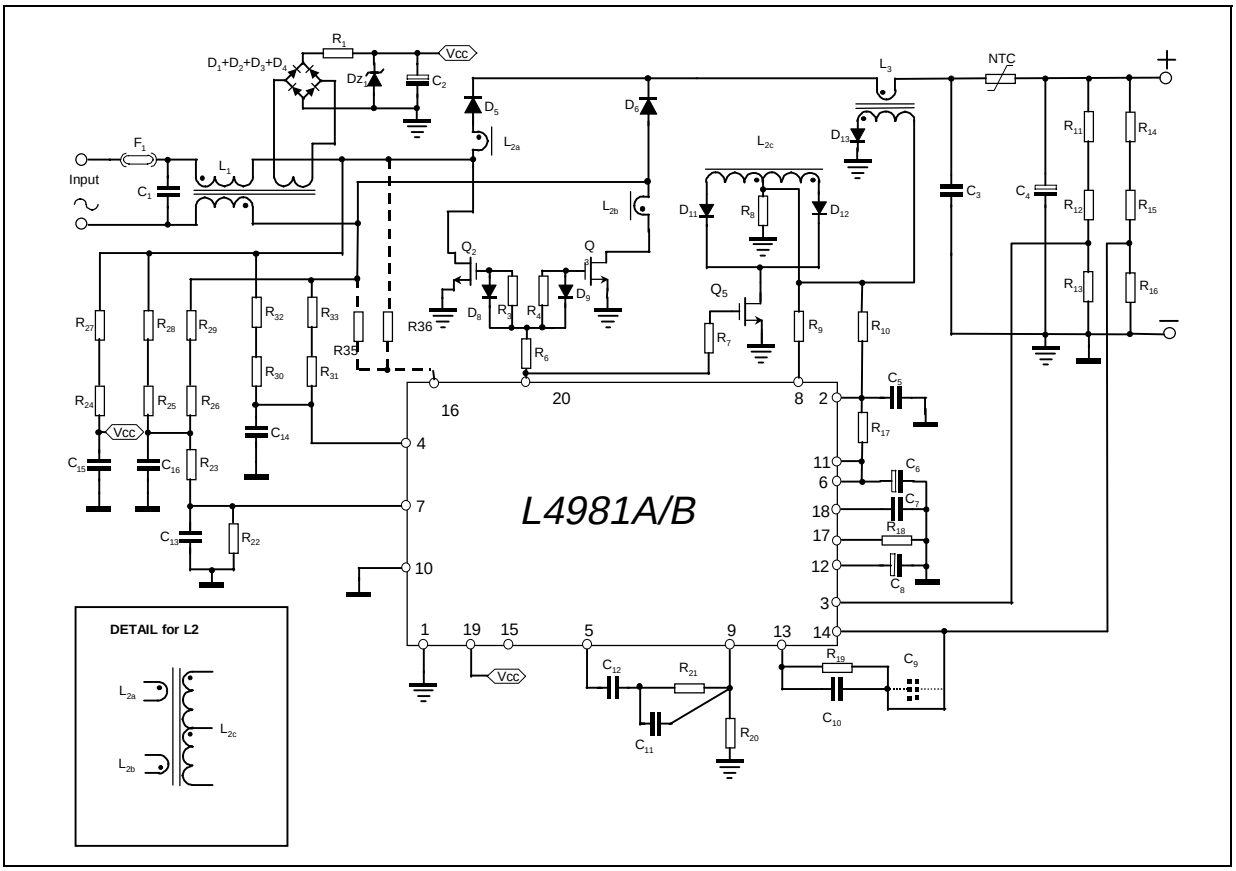
Output Capacitor.

For the selection of C_O, the relation as been described in (m). The commercial value = 330µF/450V used for the 800W application is still good for the 600W application.

Power Devices.

For the two boost diodes, as for the 800W application, the STTH8R06FP has been used.
Concerning the Powermos, the devices used in the 600W version application are two STW26NM50F.

Figure 11. 600W SCHEMATHIC DIAGRAM.



B.O.M. for 600W version Bridgeless Evaluation Circuit.

Name	Value	Name	Value	Name	Value	Name	Value	Name	Value
R_1	68 Ω	$R_{3,4}$	10 Ω	R_6	6.8 Ω	R_7	100 Ω	R_8	6.8 Ω
R_9	2.7 kΩ	R_{10}	1.5 kΩ	$R_{11,12,14,15}$	1 MΩ	R_{13}	22 kΩ	R_{16}	25.5 kΩ
R_{17}	3.9kΩ	R_{18}	33 kΩ	R_{19}	220 kΩ	R_{20}	2.7 kΩ	R_{21}	5.6 kΩ
$R_{22,24,27}$	30 kΩ	$R_{23,30,31,32,33}$	150 kΩ	$R_{25,26,28,29}$	499 kΩ	R_{34}	12 kΩ		
$C_{1,3}$	1 µF	C_2	220 µF	C_4	330 µF	C_5	10 nF	C_6	1 µF
C_7	1.8 nF	C_8	1 µF	C_{10}	120 nF	C_{11}	1 nF	C_{12}	5.6 nF
C_{13}	470 nF	C_{14}	2.7 nF	C_{15}	100 nF	C_{16}	390 nF		
NTC	2.5	B	57364			F1	15 A		

$L_{2,\#(1/50+50)}$# sense transformer ; $L_{3\#(1/50)}$# sense transformer

#Ferrites Hy_perm.' Diam.=20mm

$D_{1,2,3,4}$ $D_{8,9,11,12,13}$ =1N4148; Dz_1=1N4746; Q_5 = BS170.

L1=440 µH; => E55*28*21-21+21 turns 2.5mm/gapped# 14 wires // m=0.4 mm each.

$D_{5,6}$ = STTH8R06FP; $Q_{2,3}$ = STW26NM50F

Note: For the evaluation circuit and external coupled inductor EMC where utilized.

The filter has been achieved as follows: -

Coupled inductor (30 + 30) turns; wire diameter = 0.8mm on a toroidal (40x16x8.5 mm): -

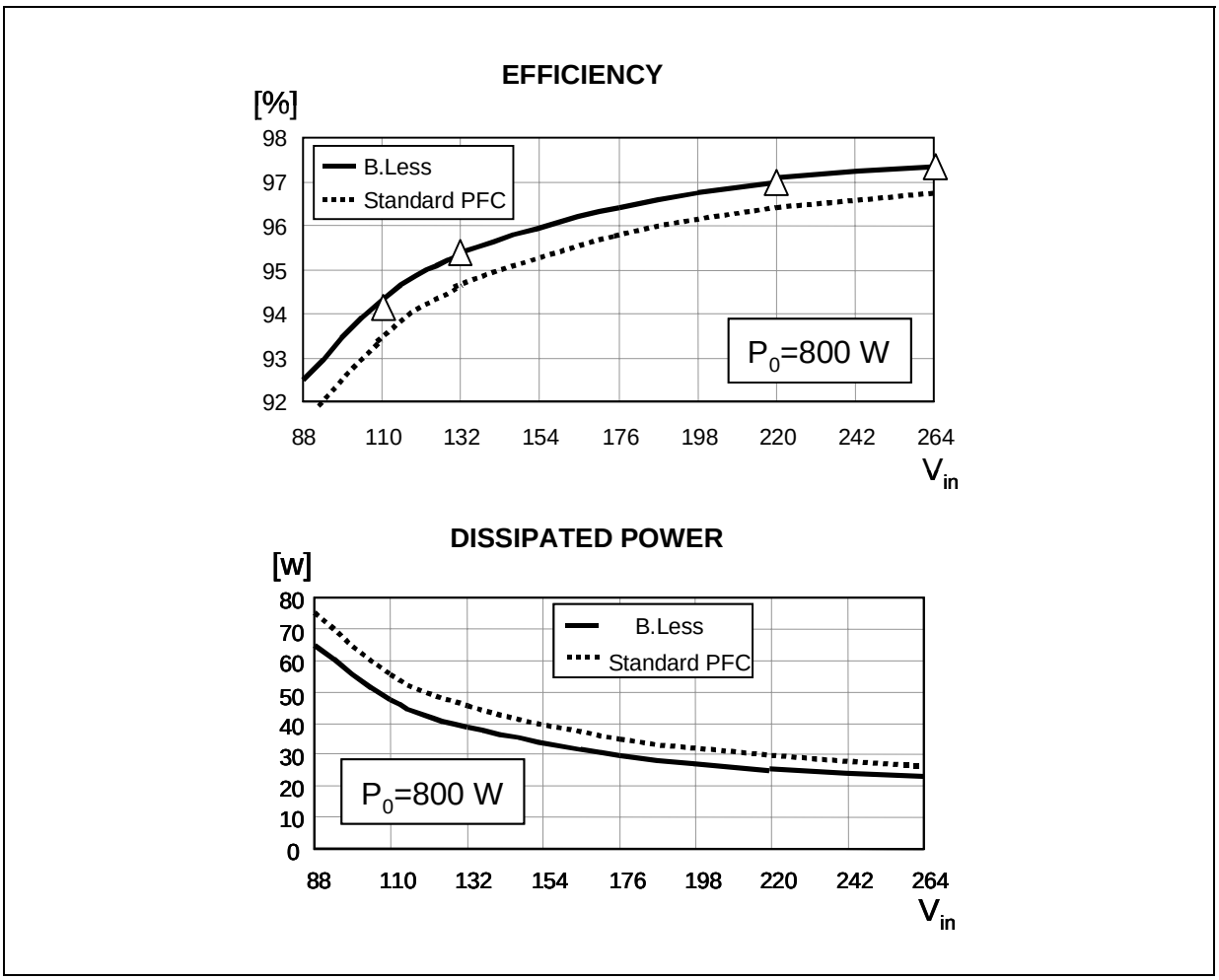
Magnetizing inductance (each half inductor) Lm=8mH and a leakage inductance, Ld=50uH.

Conclusion:

The innovative bridgeless PFC configuration as described in this application note has been successfully tested. Details have been presented how to implement the technology, which should prove interesting to designers.

Figure 12 shows the test results of efficiency and power dissipation for the application's 800W prototype.

Figure 12.



Evaluation results for the 800W version.

@Vin=110Vac: Nominal power					
Vout	**Pout**	**Pin**	**PF**	**TDH**	**Efficiency**
395VDC	800W	860W	0.999	4	94%
@Vin=220Vac: Nominal power					
395VDC	800W	824W	0.997	8	97%

Evaluation results for the 600W version.

@Vin=110Vac: Nominal power					
Vout	**Pout**	**Pin**	**PF**	**TDH**	**Efficiency**
395VDC	652W	700W	0.998	6.7	93%
@Vin=220Vac: Nominal power					
395VDC	652W	624W	0.994	9	96.5%

References: -

a) Parsad N. Enjeti, R. Martinez "A high performance single phase AC to DC rectifier with input power factor correction" IEEE APEC'93

b) Alexandre Ferrari de Souza and Ivo Barbi "A new ZVS Semi resonant High Power Factor Rectifier with Reduced Conduction Losses"

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c) STM Application Notes AN628; AN824.

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